REMARKS

The Examiner's Office Action of September 8, 2003 has been received and its contents reviewed. Applicants would like to thank the Examiner for the consideration given to the above-identified application.

Claims 6-10, and 12-14, and 21-24 are pending for consideration, of which claim 6 is independent. By this Amendment, claims 6 and 7 have been amended. In view of these actions and the following remarks, reconsideration of this application is now requested.

Claims 6-10, 12-14 and 20-24 stand rejected under 35 U.S.C. § 103(a) as unpatentable over G.G. Shahidi et al., *High Performance Devices for a 0.15 μm CMOS Technology* (hereafter Shahidi), in view of Burr (U.S. Patent No. 5,923,987 – hereafter Burr). Further, claim 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Shahidi and Burr, as applied to claim 6 above, and further in view of Tsukamoto (U.S. Patent No. 5,399,506 – hereafter Tsukamoto). These rejections are respectfully traversed at least for the reasons provided below.

As amended, claim 6 includes, among other features: a) a second step of implanting heavy ions into the semiconductor region on both sides of the gate electrode using the gate electrode as a mask, thereby forming the first ion implanted layer of the second conductivity, at least upper part of which is the amorphous layer, a dislocation loop layer is formed in the lower region of the amorphous layer in the semiconductor region due to the heavy ions implantation; and b) a fourth step of conducting the first annealing process to activate the first and second ion implanted layers, thereby forming the extended high-concentration dopant diffused layer of the first conductivity type through diffusion of the first dopant and the pocket dopant diffused layer of the second conductivity type, which is in contact with the bottom portion of the extended high-concentration dopant diffused layer, through diffusion of the heavy ions, respectively, the pocket dopant diffused layer including the part in which the heavy ions are trapped is formed in the dislocation loop layer.

Hence, according to the amended claim 6 and as illustrated in an attached Fig. C, which is based on Fig. 4b in the present specification, during the first annealing process in which the first and second ion implanted layers are activated, the part (1) of the dislocation loop layer in which heavy ions are trapped is formed in the pocket dopant diffused layer (A). Accordingly, since the first dopant for forming the extended high-concentration dopant

diffused layer is implanted after forming the first ion implanted layer, in which upper part is an amorphous layer, by heavy ions implantation, the channeling of the first dopant can be suppressed.

In addition, since silicon interstitials that cause transient enhanced diffusion (TED) are being trapped in the dislocation loop layer, resulting in a decrease in quantity due to the first annealing process, the transient enhanced diffusion of the heavy ions is suppressed.

Moreover, since the heavy ions are being trapped and segregated in the dislocation loop layer, diffusion of significant amount of heavy ions to the low concentration region of the pocket dopant diffused layer (the tail portion of the dopant profile) is suppressed, and, as a result, the extended high-concentration dopant diffused layer can have a shallow and sharp junction.

Turning to the cited references, Shahidi fails to disclose a pocket dopant diffused layer including a part of the dislocation loop layer in which indium ions are trapped. Moreover, as illustrated in an attached Fig. D, which is based on Fig. 1b in Shahidi, neither a dislocation loop layer nor a part of a dislocation loop layer in which indium ions are trapped is provided in the pocket dopant diffused layer (B).

With respect to Burr, the reference teaches: a) forming a pocket region (347) by ion implanting p-type ions, such as boron or indium, into a drain using a gate electrode (342) and a mask (326) as a mask; b) thereafter, forming n doped layers (336A, 338A) by ion implanting n-type ions, such as P, As, Sb or Sn, using the gate electrode (342) as a mask; and c) thereafter performing a heat treatment. However, Burr fails to disclose forming an amorphous layer in the upper part of the pocket region (347) by ion implanting p-type ions or forming a dislocation loop layer. Hence, Burr fails to teach or suggest that, after the heat treatment, the pocket dopant diffused layer (347) includes a part of a dislocation loop layer in which p-type ions are trapped.

In addition, as disclosed in lines 38-55 of column 14 of Burr, the implanted dosage of the pocket region (347) is between 5×10^{11} and 1×10^{13} cm^{-2}. With such a range of dosage, even if indium ions are being implanted, an amorphous layer and a dislocation loop layer would not be formed.

For the foregoing reasons, both Shahidi and Burr fail to teach or suggest the step of forming the dislocation loop layer during the implantation of heavy ions for forming the

pocket region, and thereafter forming the pocket region having the shallow junction by performing the annealing process for trapping the heavy ions in the dislocation loop layer, as recited in amended claim 6. Hence, the amended claim 6, as well as its dependent claims, is distinguishable over the combination of Shahidi and Burr.

In view of the amendments and arguments set forth above, Applicants respectfully requests reconsideration and withdrawal of the pending § 112, first paragraph, and the §103(a) rejections.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise which could be eliminated through discussions with Applicants' representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby be expedited.

Respectfully submitted,

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ATTACHMENT

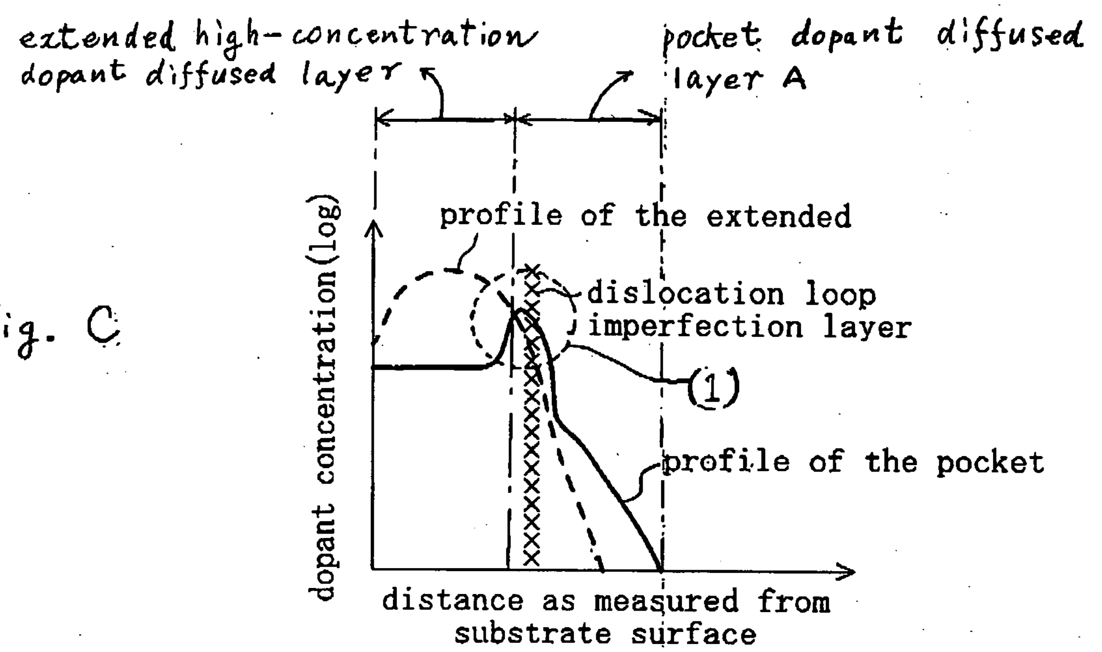

Fig. C

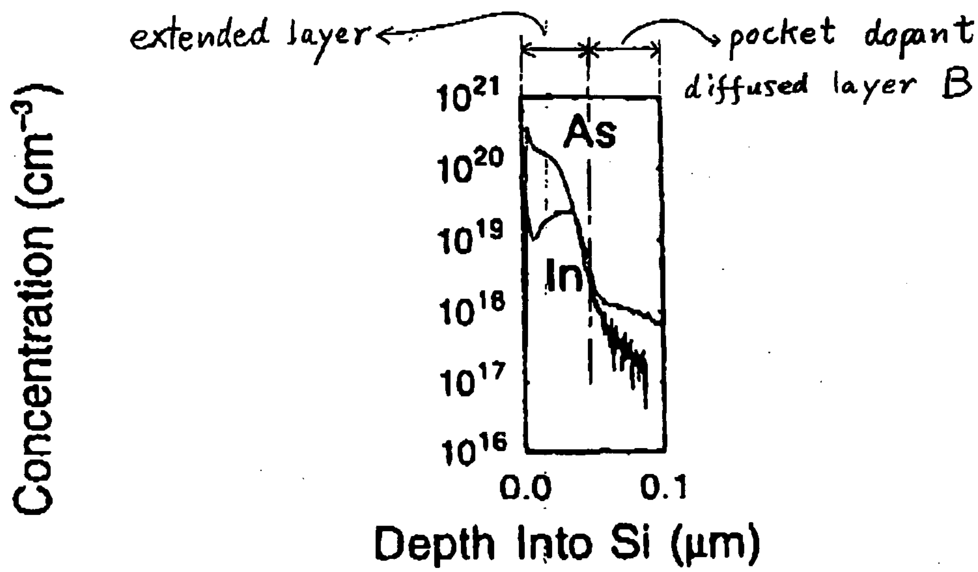

Fig. D